Abstract

The invention relates to a pulse width modulator circuit for generating a reference signal having a desired duty cycle comprising an adjustment unit including at least one storage register and a counter, the storage register being configured for storing values corresponding to the desired duty cycle at least approximately and which are set during a working cycle in the pulse width modulator circuit for generating a reference signal, and the counter seting a cycle count Y indicating how often a stored first value X is read during the working cycle A from the storage register, the value stored in the storage register being variable during the working cycle.